IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent application of :

Min Kim et al. : **BOX NEW APPLICATIONS**

Serial No. (new) :

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TRENCH ISOLATION STRUCTURE HAVING A CURVILINEAR INTERFACE AT UPPER CORNERS OF THE TRENCH ISOLATION REGION, AND METHOD OF MANUFACTURING THE SAME

PRELIMINARY AMENDMENT

Honorable Commissioner For Patents
Washington, D.C. 20131

Sir:

Prior to the examination of the above-identified application, the following amendments and remarks are submitted:

In the Specification[1]

Kindly amend the paragraph [0100] to read as follows:

[0100] FIG. 6 shows a first embodiment of trench isolation structure in which a trench 116 extends into a semiconductor substrate 104 from an upper surface of the substrate, and a trench isolation layer occupies the trench to electrically isolate active

[1] A copy of any revised paragraphs/sections of the specification showing additions and deletions thereto is attached as ATTACHMENT "A".

regions. In this embodiment, the trench isolation layer comprises a first oxide layer 120b, a buffer layer 118a, and a thermal oxide layer 114a. The first oxide layer 120b is buried in the trench 116 of the semiconductor substrate 104 as surrounded by the buffer layer 118a. The thermal oxide layer 114a contacts the buffer layer 118a at the upper corners of the substrate 104 where the upper surface of the substrate 104 and inner walls of the substrate 104 that define the trench 116 meet. Thus, the trench isolation layer and the semiconductor substrate contact each other at the upper corners of the substrate 104. This interface between the trench isolation layer and the semiconductor substrate has a rounded vertical sectional profile. More specifically, the interface between the thermal oxide layer 114a and the semiconductor substrate 104 has a rounded, i.e., curvilinear, vertical sectional profile.

Kindly amend the paragraph [0145] to read as follows:

[0145] An oxide layer such as an HTO oxide layer, a MTO layer or a PE-oxide layer is formed over the resulting structure. Then the resulting structure is anisotropically etched to form a spacer 110 along the sidewall of the hard mask pattern 108 and the pad oxide pattern 106. Of course, it is possible to perform a subsequent step without forming the spacer 110. In the embodiment, a method of manufacturing a trench isolation layer, in which a subsequent step is performed after having formed the spacer 110, will now be described.

Kindly amend the paragraph [0150] to read as follows:

[0150] Referring now to FIG. 9, using the hard mask pattern 108 and the spacer 110 as a mask, a shallow trench 112 is formed in a portion of the semiconductor substrate 104. The shallow trench 112 is preferably formed within the monocrystalline silicon layer 102 itself, i.e. does not extend down to the buried oxide layer.

Kindly amend the paragraph [0180] to read as follows:

[0180] FIGS. 15 and 16 show the key steps in another embodiment of a method of manufacturing a trench isolation layer according to the present invention. Referring to FIG. 15, a pad oxide layer and a hard mask layer are sequentially deposited over a semiconductor substrate 204 and patterned to form a hard mask pattern 208 and a pad oxide pattern 206, and to expose a portion of the upper surface of the semiconductor substrate. Next, a spacer 210 is formed along the sidewalls of the hard mask pattern 208 and a pad oxide pattern 206. As in the first embodiment, the spacer 210 does not need to be formed. Thus, a subsequent step may be performed without forming the spacer 201.

Kindly amend the paragraph [0185] to read as follows:

[0185] Subsequently, a thermal oxide layer 214 is formed on the exposed portion of the upper surface of the semiconductor substrate 204. That is, the portion of the semiconductor substrate 204 at which the isolation layer will be formed is subjected to thermal oxidation. Hence, an oxide layer grows from the exposed surface of the

semiconductor substrate 204, thereby forming a thermal oxide layer 214 that extends to a location beneath the spacer 210/hard mask pattern 208. In this case, the peripheral portion of the thermal oxide layer 214 has the shape of a bird's beak.

Kindly amend the paragraph [0190] to read as follows:

[0190] Referring to FIG. 16, the thermal oxide layer 214 and the semiconductor substrate 204 are etched using the hard mask pattern 208 and the spacer 210 as a mask, to thereby form a deep trench 216. The peripheral portion of the thermal oxide layer 214 remains as protected by the spacer 210/hard mask pattern 208. The deep trench 216 is formed down to the interface between the monocrystalline silicon layer 202 and the buried oxide layer 201. Alternatively, the deep trench 216 may be formed down to the interface between the buried oxide layer 201 and the silicon substrate 200. Forming the deep trench 216 in this way leaves the peripheral portion of the thermal oxide layer 214a that has the shape of a bird's beak. That is, the interface between the remaining portion of the thermal oxide layer 212 and the semiconductor substrate 204, at the upper corners of the substrate 204 where the trench 216 begins, has a vertical sectional profile in the shape of a rounded bird's beak as shown in FIG. 16.

REMARKS

By this Preliminary Amendment, the specification has been revised to correct minor errors of a typographical and grammatical nature and to generally improve the clarity thereof. No new matter has been added.

Entry of this Preliminary Amendment is respectfully requested.

Respectfully submitted,

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ATTACHMENT "A"

Additions/Deletions to the Specification:

[0100] FIG. 6 shows a first embodiment of trench isolation structure in which a trench 116 extends into a semiconductor substrate 104 from an upper surface of the substrate, and a trench isolation layer occupies the trench to electrically isolate active regions. In this embodiment, the trench isolation layer comprises a first oxide layer 120b, a buffer layer 118a, and a thermal oxide layer 114a. The first oxide layer 120b is buried in the trench 116 of the semiconductor substrate 104 as surrounded by the buffer layer 118a. The thermal oxide layer 114a contacts the buffer layer 118a at the upper corners of the substrate 104 where the upper surface of the substrate 104 and inner walls of the substrate 104 that define the trench 116 meet. Thus, the trench isolation layer and the semiconductor substrate contact each other at the upper corners of the substrate 104. This interface between the trench isolation layer and the semiconductor substrate has a rounded vertical sectional profile. More specifically, the interface between the thermal oxide layer 114a and the semiconductor substrate 104 has a rounded, i.e., curvilinear, vertical sectional profile.

[0145] An oxide layer such as an HTO oxide layer, a MTO layer or a PE-oxide layer is formed over the resulting structure. Then the resulting structure is anisotropically etched to form a spacer 110 along the sidewall of the hard mask pattern 108 and the pad oxide pattern 106. [~~However, the spacer 110 can be formed at later stages of the process.~~] Of course, it is possible to perform a subsequent step without

forming the spacer 110. In the embodiment, a method of manufacturing a trench isolation layer, in which a subsequent step is performed after having formed the spacer 110, will now be described.

[0150] Referring now to FIG. 9, using the hard mask pattern 108 and the spacer 110 as a mask, a shallow trench 112 is formed in a portion of the semiconductor substrate 104. The [~~shall~~] shallow trench 112 is preferably formed within the monocrystalline silicon layer 102 itself, i.e. does not extend down to the buried oxide layer.

[0180] FIGS. 15 and 16 show the key steps in another embodiment of a method of manufacturing a trench isolation layer according to the present invention. Referring to FIG. 15, a pad oxide layer and a hard mask layer are sequentially deposited over a semiconductor substrate 204 and patterned to form a hard mask pattern 208 and a pad oxide pattern 206, and to expose a portion of the upper surface of the semiconductor substrate. Next, a spacer 210 is formed along the sidewalls of the hard mask pattern 208 and a pad oxide pattern 206. As in the first embodiment, the spacer 210 does not need to be formed [~~at this stage of the process~~]. Thus, a subsequent step may be performed without forming the spacer 201.

[0185] Subsequently, a thermal oxide layer [~~212~~] 214 is formed on the exposed portion of the upper surface of the semiconductor substrate 204. That is, the portion of

the semiconductor substrate 204 at which the isolation layer will be formed is subjected to thermal oxidation. Hence, an oxide layer grows from the exposed surface of the semiconductor substrate 204, thereby forming a thermal oxide layer [~~212~~] 214 that extends to a location beneath the spacer 210/hard mask pattern 208. In this case, the peripheral portion of the thermal oxide layer [~~212~~] 214 has the shape of a bird's beak.

[0190] Referring to FIG. 16, the thermal oxide layer [~~212~~] 214 and the semiconductor substrate 204 are etched using the hard mask pattern 208 and the spacer 210 as a mask, to thereby form a deep trench 216. The peripheral portion of the thermal oxide layer [~~212~~] 214 remains as protected by the spacer 210/hard mask pattern 208. The deep trench 216 is formed down to the interface between the monocrystalline silicon layer 202 and the buried oxide layer 201. Alternatively, the deep trench 216 may be formed down to the interface between the buried oxide layer 201 and the silicon substrate 200. Forming the deep trench 216 in this way leaves the peripheral portion of the thermal oxide layer 214a that has the shape of a bird's beak. That is, the interface between the remaining portion of the thermal oxide layer 212 and the semiconductor substrate 204, at the upper corners of the substrate 204 where the trench 216 begins, has a vertical sectional profile in the shape of a rounded bird's beak as shown in FIG. 16.